

Figure 1

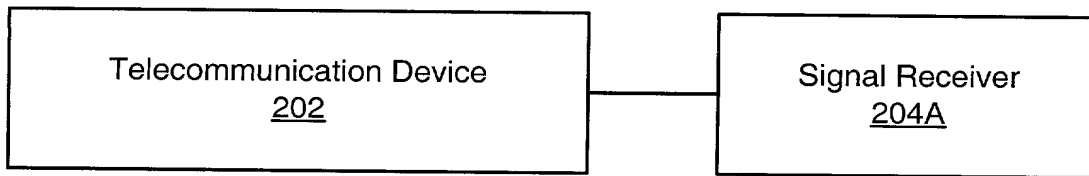


Figure 2A

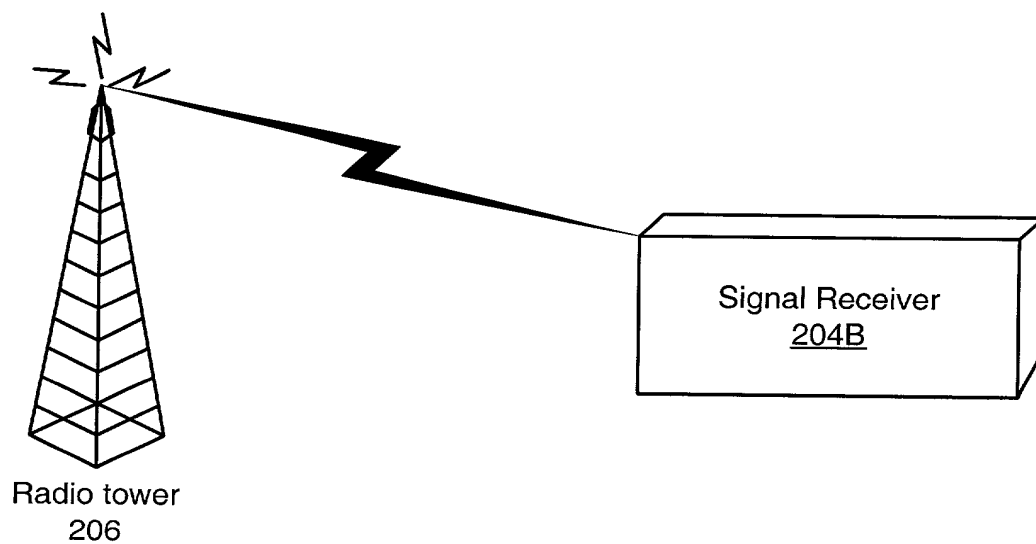


Figure 2B

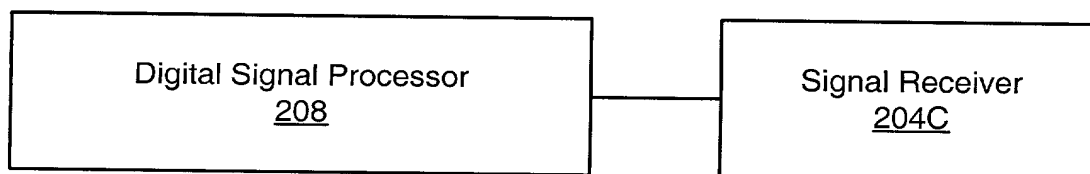


Figure 2C

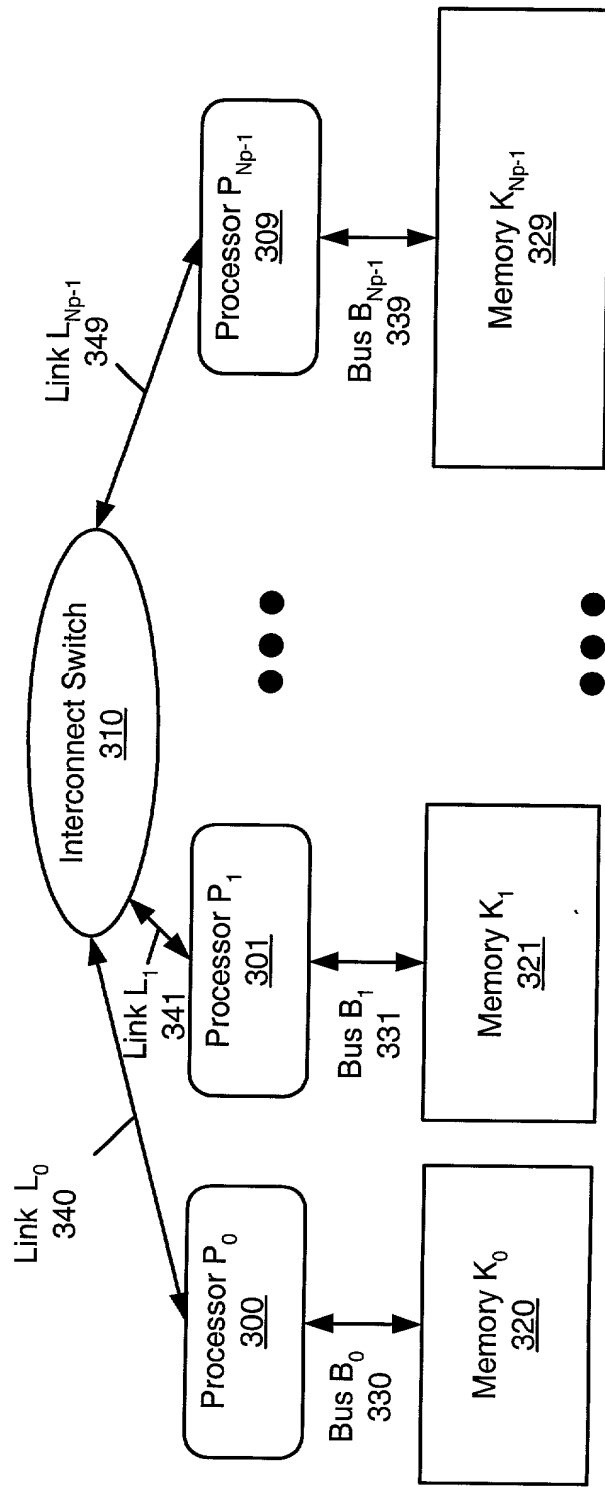


Figure 3

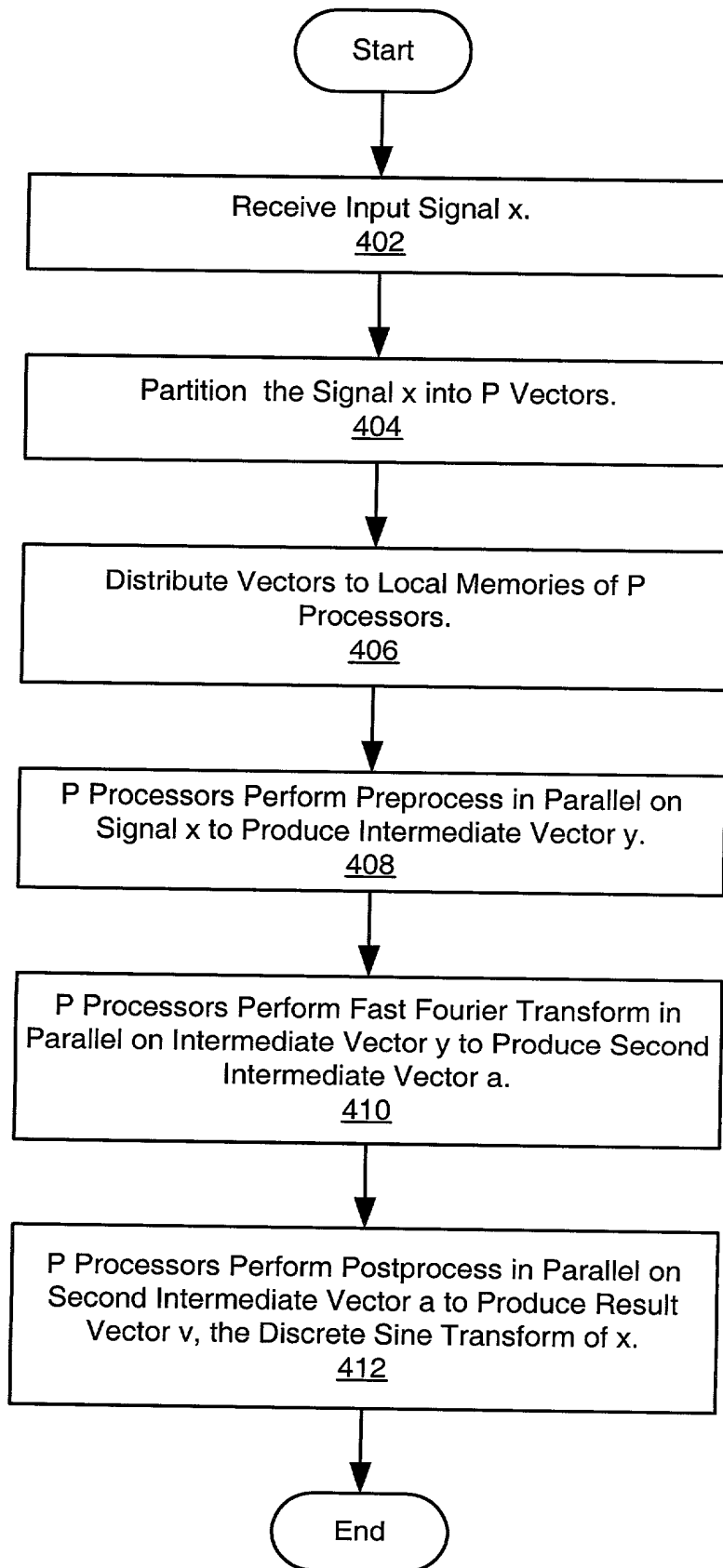


Figure 4A

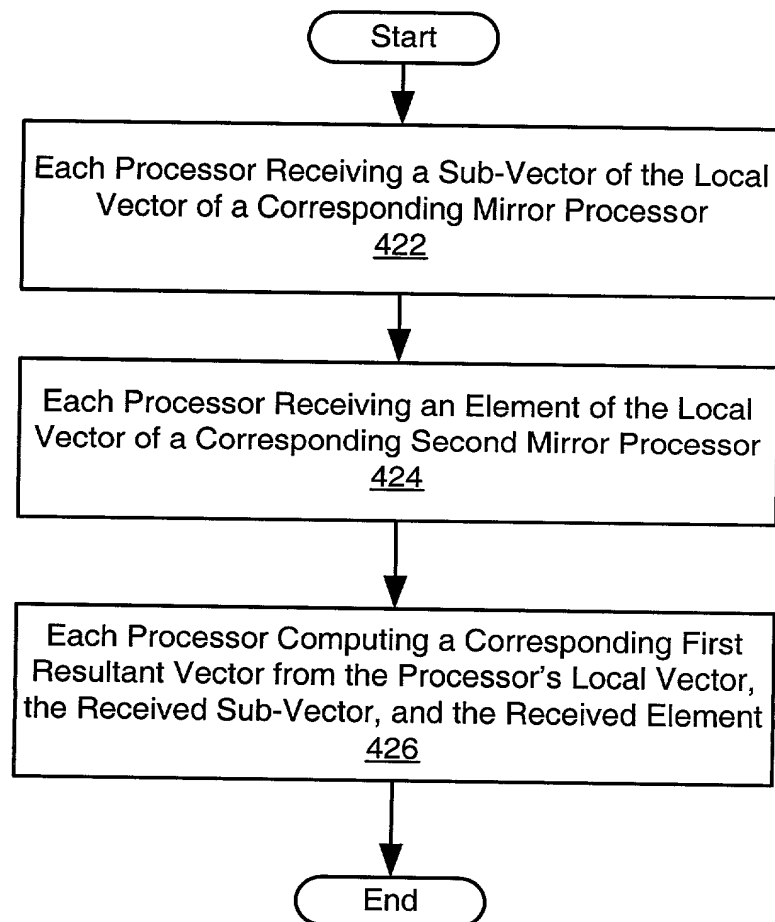


Figure 4B

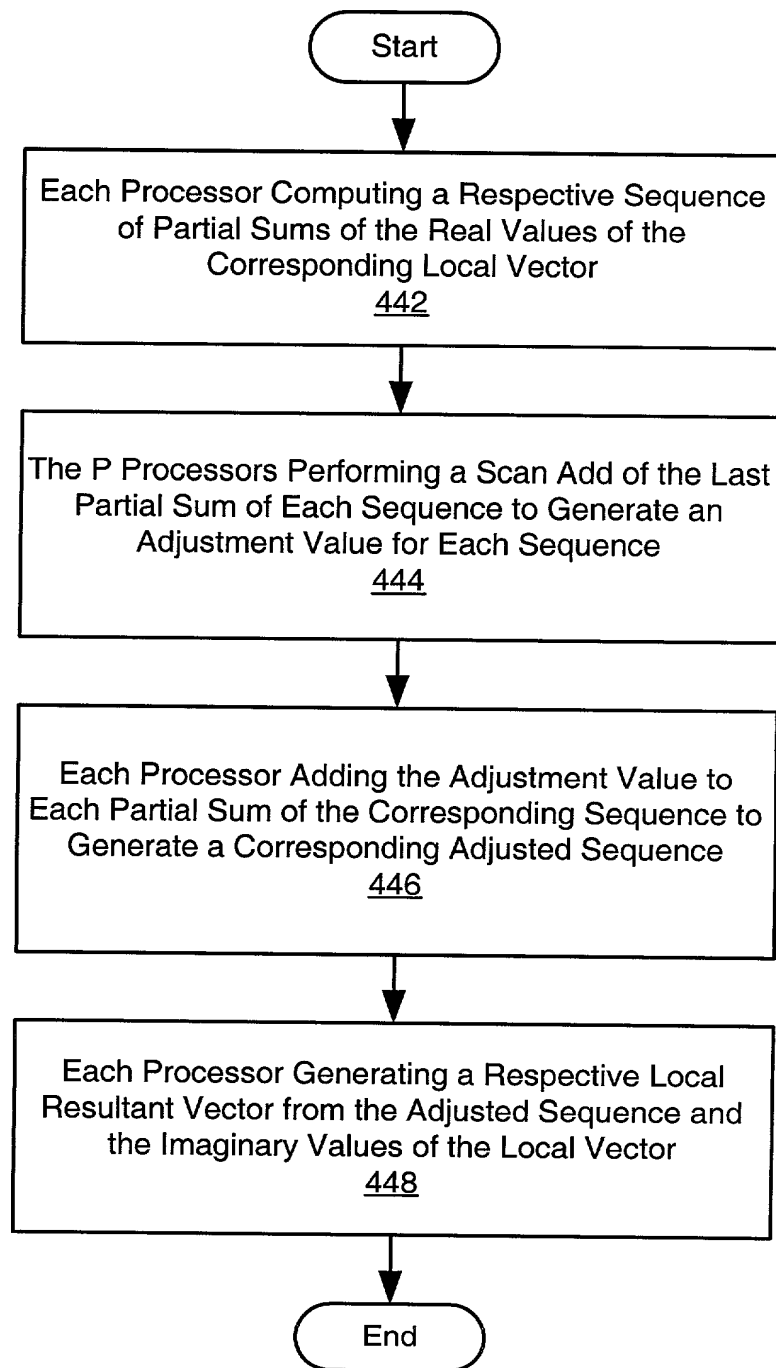


Figure 4C

FIG. 5A is a diagram illustrating a data distribution process. It shows a sequence of memory blocks (K0, K1, K2, K3) and a buffer (Buf1) connected by arrows indicating data flow. The memory blocks are labeled P0, P1, P2, and P3. The buffer is labeled Buf1. The data is distributed from the memory blocks to the buffer in a specific order.

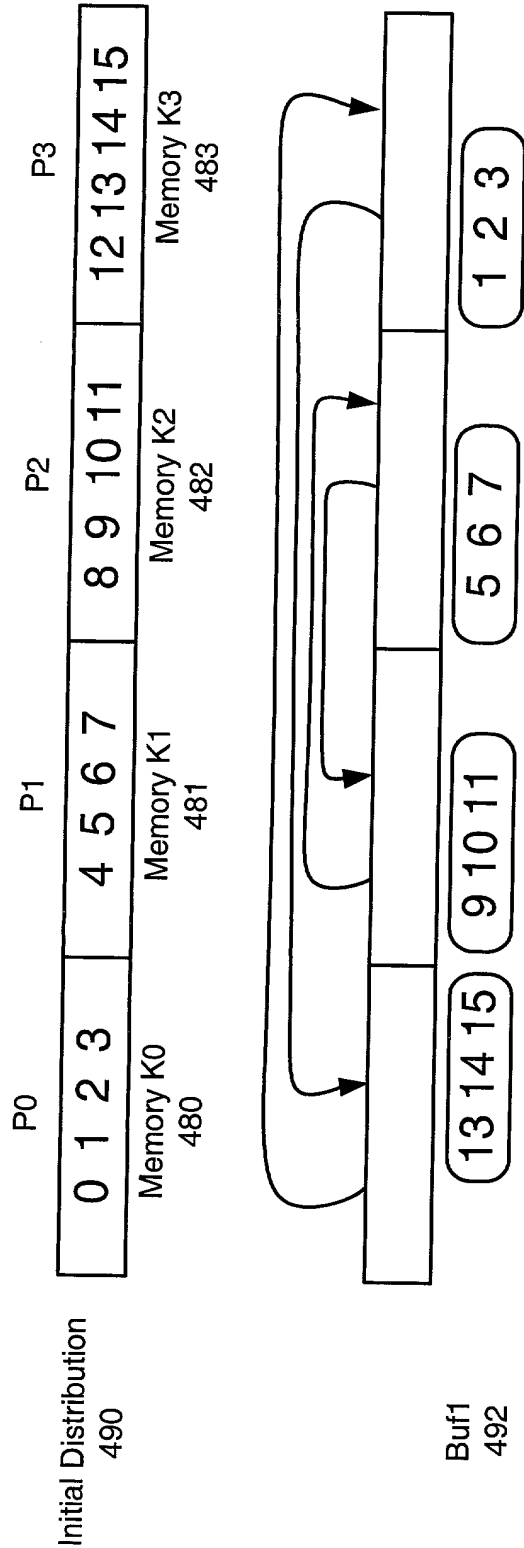


Figure 5A

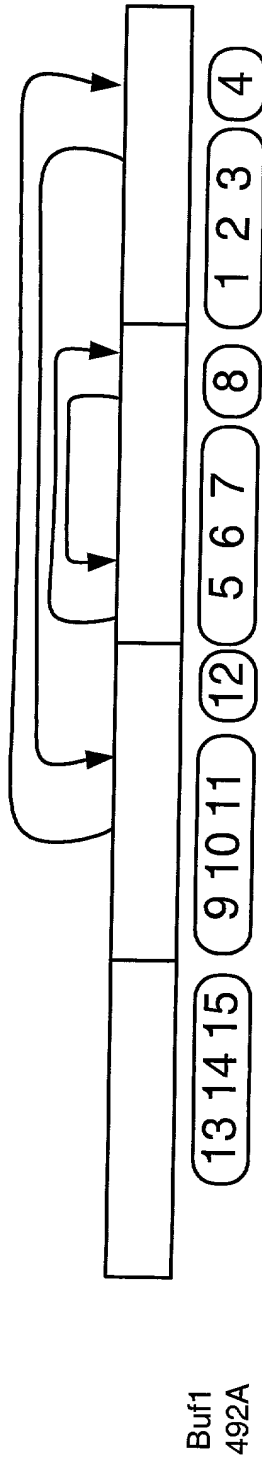


Figure 5B

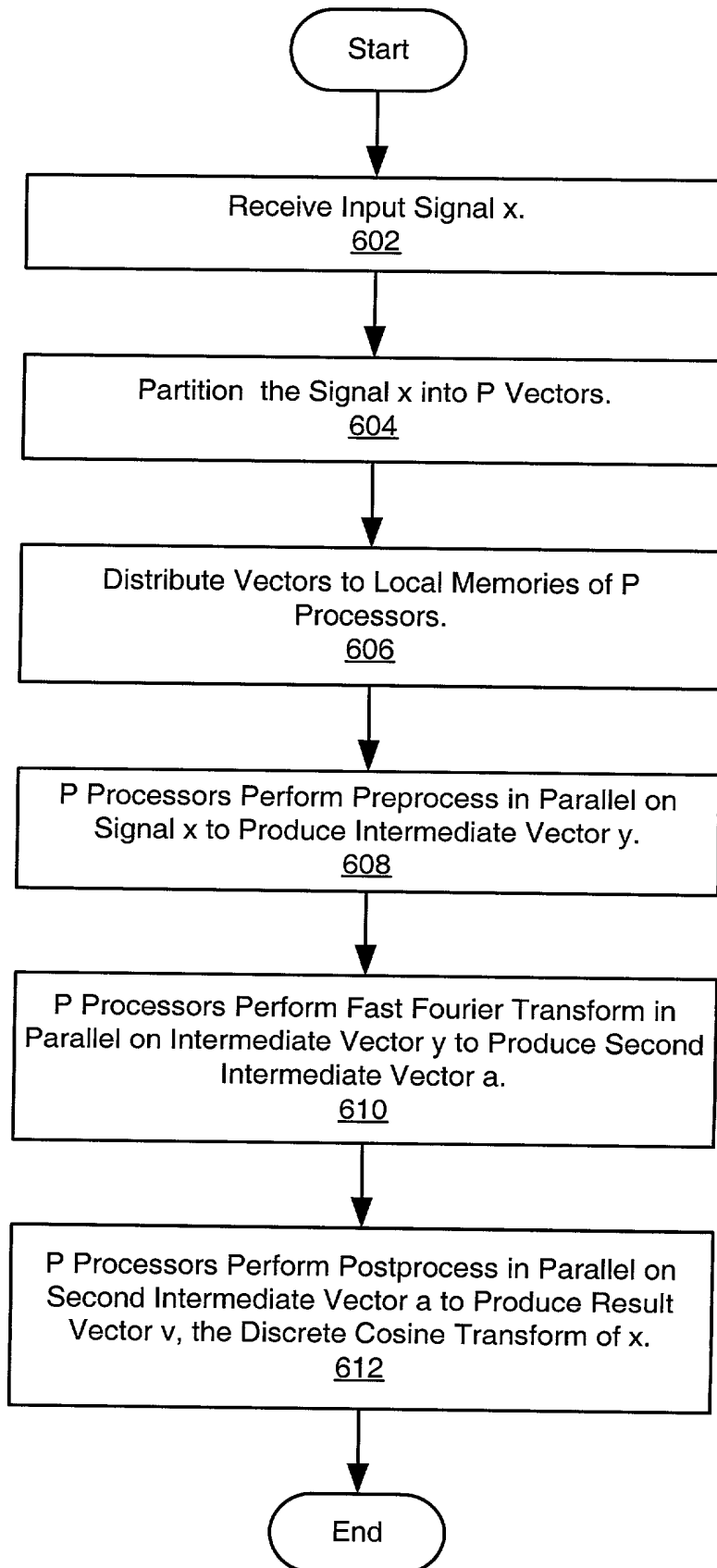


Figure 6A



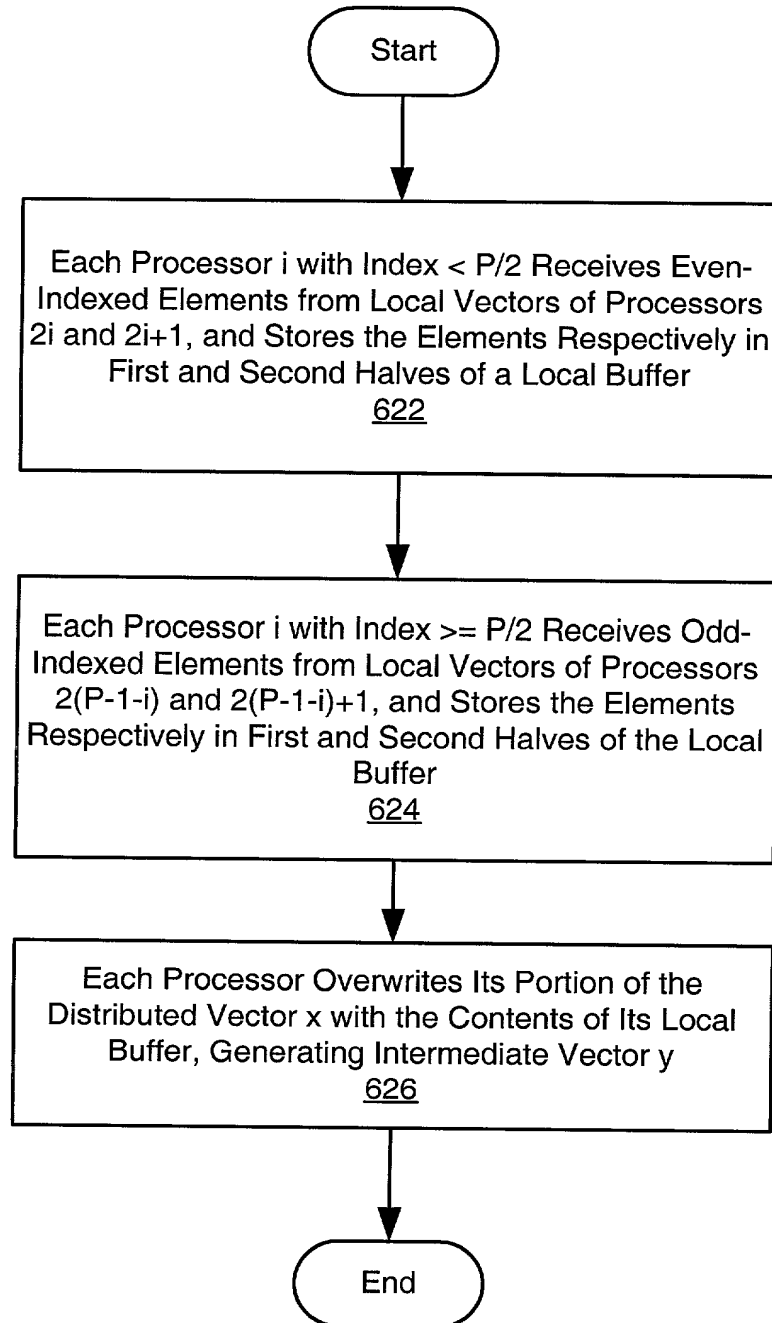


Figure 6B

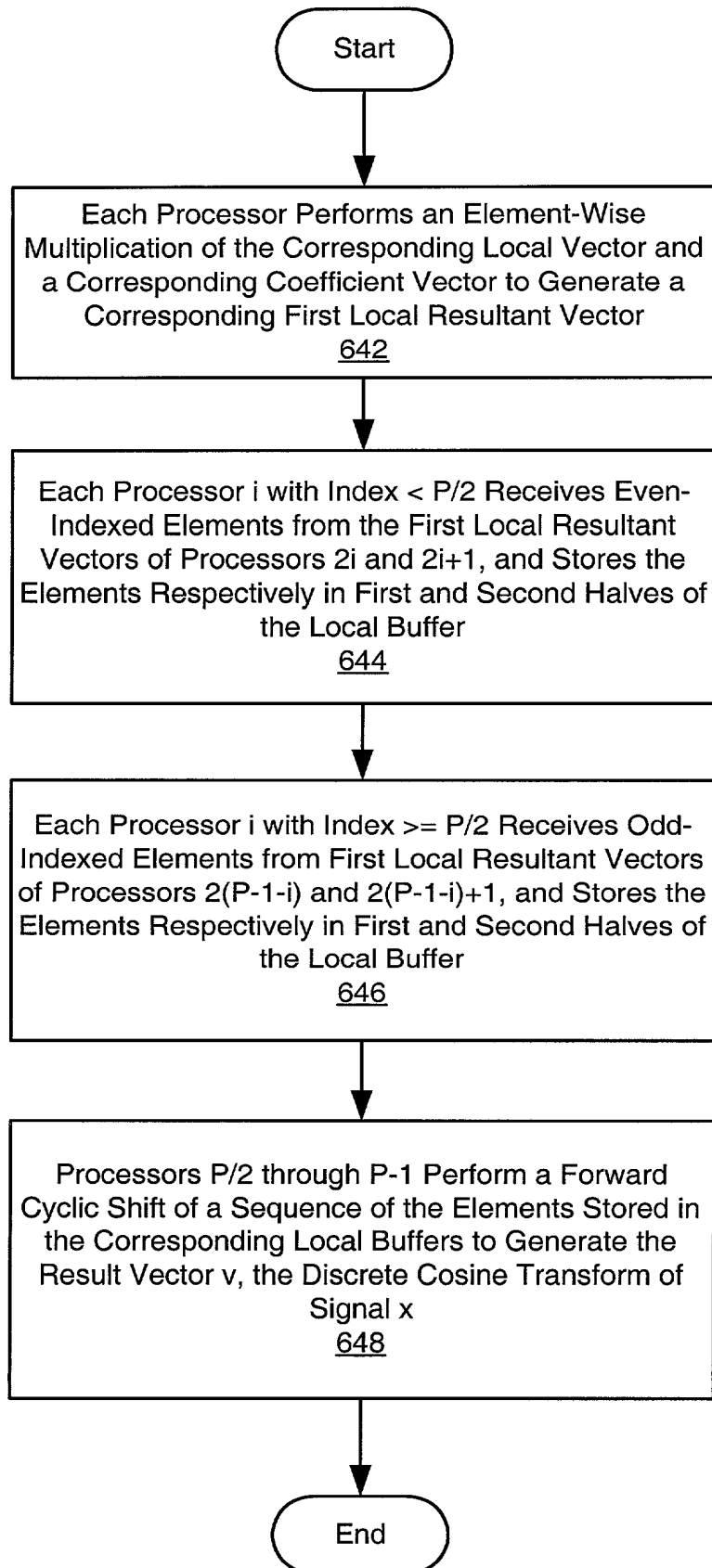


Figure 6C